EXPERIMENT NO. 7: DIFFERENTIAL AMPLIFIER AND BASIC OP-AMP GAIN STAGES

1.0 AIM:

The primary aim of this experiment is to thoroughly analyze the DC and AC performance characteristics of a Bipolar Junction Transistor (BJT) differential amplifier, specifically focusing on its differential gain, common-mode gain, and Common Mode Rejection Ratio (CMRR). Furthermore, the experiment aims to explore and characterize the fundamental gain stages of an Operational Amplifier (Op-Amp) in both inverting and non-inverting configurations.

2.0 OBJECTIVES:

Upon successful completion of this experiment, you will be able to:

- **Understand Differential Amplifier Principles: Grasp the fundamental operation of a differential amplifier, including its response to differential and common-mode input signals.**
- **Construct BJT Differential Amplifier: Build a basic BJT differential amplifier circuit using discrete components, incorporating a constant current source (or a simple resistor approximation).**
- **Measure Differential Gain (Ad): Experimentally determine the differential voltage gain of the BJT differential amplifier.**
- **Measure Common-Mode Gain (Acm): Experimentally determine the common-mode voltage gain of the BJT differential amplifier.**
- **Calculate CMRR: Compute the Common Mode Rejection Ratio (CMRR) in decibels (dB) from measured gains, and understand its significance.**
- **Determine Input Common Mode Range (ICMR): Identify the range of common-mode input voltages over which the differential amplifier maintains linear operation.**
- **Implement Op-Amp Basic Stages: Construct and test basic inverting and non-inverting amplifier configurations using a general-purpose Op-Amp (e.g., LM741).**
- **Measure Op-Amp Gain and Bandwidth: Experimentally measure the voltage gain and bandwidth of both inverting and non-inverting Op-Amp configurations.**
- **Understand Op-Amp Internal Stages: Conceptually identify and explain the roles of the input differential stage, intermediate gain stages, and output stage within a typical Op-Amp architecture.**
- **Instrumentation Skills: Effectively utilize essential laboratory equipment such as DC power supply, AC function generator, oscilloscope, and DMM for circuit characterization.**

3.0 APPARATUS REQUIRED:

A comprehensive list of components and equipment necessary for performing this experiment.

S. No.	Component/Equipment	Specifications/Value	Quantity
1.	DC Power Supply (Variable)	Dual Output (e.g., +/- 15V, or 0-30V)	1
2.	AC Function Generator	Sine wave, Adjustable Amplitude, Wide Frequency Range (10Hz-1MHz)	1
3.	Digital Multimeter (DMM)	Multi-function (Voltage, Current, Resistance)	1
4.	Oscilloscope	Dual Trace, Minimum 20MHz Bandwidth	1
5.	Breadboard	Standard Size, for circuit prototyping	1
6.	NPN Bipolar Junction Transistors	BC547 (matched pair if possible, i.e., similar Beta)	2
7.	NPN BJT (for current source)	BC547 (or similar, for constant current source)	1
8.	Operational Amplifier (Op-Amp)	LM741 (or equivalent general-purpose Op-Amp)	1

9.	Resistors (Carbon Film, 1/4W)	Various values (1 kΩ, 2.2 kΩ, 4.7 kΩ, 10 kΩ, 22 kΩ, 100 kΩ)	Assorted
10.	Capacitors (Ceramic/Electrolytic)	Coupling Capacitors: 0.1 µF, 1 µF (for Op-Amp BW test)	Assorted
11.	Connecting Wires	Breadboard jumper wires, various lengths	Assorted

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4.0 THEORY AND FUNDAMENTALS:

This section provides a detailed theoretical background for differential amplifiers and Op-Amp gain stages, including necessary formulas and explanations for a thorough understanding.

4.1 The BJT Differential Amplifier

A differential amplifier is a fundamental building block in many analog circuits, particularly in operational amplifiers. Its key characteristic is its ability to amplify the difference between two input signals while largely rejecting signals common to both inputs.

4.1.1 Basic Operation and Circuit Structure

- **A basic BJT differential amplifier consists of two matched transistors (Q1 and Q2) with their emitters connected together to a common current source. The inputs are applied to the bases of Q1 (V_{in1}) and Q2 (V_{in2}), and the outputs are typically taken from the collectors (V_{out1} and V_{out2}).**
- **Common Current Source (or Emitter Resistor): The constant current source (or a large resistor R_E connected to a negative supply) at the common emitter point is crucial. It ensures that the total emitter current ($I_E=I_{E1}+I_{E2}$) remains constant. This constant current is then split between the two transistors. When a differential input is applied, the current shifts between Q1 and Q2, while the total current remains constant, enabling differential amplification. A simple large resistor connected to a negative supply can approximate a current source.**
- **Dual-Ended Output: Output can be taken from one collector to ground (single-ended output) or between the two collectors (differential output). For this experiment, we'll generally consider single-ended outputs for gain measurements.**

4.1.2 Input Signal Modes

A differential amplifier responds to two types of input signals:

- **Differential-Mode Input (V_id): The difference between the two input signals. V_id=V_in1−V_in2**
- **Common-Mode Input (V_ic): The average of the two input signals. V_ic=fracV_in1+V_in22**

Any arbitrary input signals V_in1 and V_in2 can be decomposed into their differential and common-mode components:

V_in1=V_ic+fracV_id2

V_in2=V_ic−fracV_id2

4.1.3 Differential Gain (A_d)

- **When a pure differential input signal (V_in1=V_id/2 and V_in2=−V_id/2) is applied, the amplifier ideally produces an amplified output.**
- **The differential gain (single-ended output from one collector, e.g., V_out1) is given by:**
  A_d=fracV_out1V_id=−fracg_mR_C2
  Where g_m is the transconductance of the transistor, and R_C is the collector resistor.
  g_m=fracI_CQV_T, where I_CQ is the quiescent collector current of each transistor (so I_CQ=I_total_current_source/2), and V_Tapprox26textmV at room temperature.
  So, A_d=−fracI_CQR_C2V_T
- **The negative sign indicates a 180-degree phase shift for the output from the collector when the corresponding input is positive.**

Numerical Example (Differential Gain):

Assume a differential amplifier with R_C=4.7kOmega. The constant current source provides 1mA, so I_CQ=0.5mA for each transistor.

V_T=26mV.

A_d=−frac(0.5textmA)times(4.7kOmega)2times(26textmV)=−frac0.5times10−3times4.7times1032times26times10−3=−frac2.350.052approx−45.19

4.1.4 Common-Mode Gain (A_cm)

- **When a pure common-mode input signal (V_in1=V_in2=V_ic) is applied, the amplifier ideally produces no output. In a real amplifier, there is a small output due to imperfections.**
- **For a differential amplifier with a current source approximated by a large emitter resistor R_E:**
  A_cm=fracV_out1V_ic=−fracR_C2R_E′
  Where R_E′ is the effective resistance seen at the common emitter point. If a BJT current source is used, R_E′ represents the output resistance of the

current source (which is typically very high). If a simple large resistor R_E is used, then R_E′=R_E.

- **Ideally, for a perfect common-mode rejection, A_cm should be zero.**

Numerical Example (Common-Mode Gain):

Assume the same differential amplifier with R_C=4.7kOmega. The common current source is approximated by a resistor R_E=100kOmega to a negative supply.

A_cm=−frac4.7kOmega2times100kOmega=−frac4.7200=−0.0235 (very small, as desired).

4.1.5 Common Mode Rejection Ratio (CMRR)

- **CMRR is a measure of a differential amplifier's ability to reject common-mode signals while amplifying differential signals. A higher CMRR indicates better rejection of common-mode noise.**
- **CMRR=frac∣A_d∣∣A_cm∣**
- **In decibels: CMRR_dB=20log_10left(frac∣A_d∣∣A_cm∣right)**
- **A good differential amplifier will have a very high CMRR (e.g., > 60 dB).**

Numerical Example (CMRR):

Using the previous examples, A_d=−45.19 and A_cm=−0.0235.

CMRR=frac∣−45.19∣∣−0.0235∣approx1923

CMRR_dB=20log_10(1923)approx20times3.28approx65.6textdB

4.1.6 Input Common Mode Range (ICMR)

- **The ICMR defines the range of common-mode input voltages over which the differential amplifier operates linearly, without saturating or cutting off either transistor.**
- **For a BJT differential amplifier, the lower limit of ICMR is constrained by the transistors entering cutoff if the common-mode input voltage becomes too low relative to the emitter voltage.**
- **The upper limit of ICMR is constrained by the transistors entering saturation if the common-mode input voltage becomes too high, causing V_CE to drop below V_CE(sat). It's also limited by the common-mode input voltage approaching the collector supply voltage.**
- **Typically, V_C,minV_B,max (for common-mode range) to ensure both transistors remain in active region.**

4.2 Operational Amplifiers (Op-Amps)

An Op-Amp is a high-gain, direct-coupled, differential input, voltage amplifier with a single-ended output. It is a versatile building block for a wide range of analog circuits due to its ideal characteristics: infinite open-loop gain, infinite input impedance, zero

output impedance, and infinite bandwidth. In reality, these are finite but still very good.

4.2.1 Internal Op-Amp Stages (Conceptual)

A typical Op-Amp (like the LM741) consists of several cascaded stages:

1. **Input Differential Stage: This is the first stage, usually a BJT or FET differential amplifier (similar to what you build in Part A). It provides high input impedance, differential gain, and excellent common-mode rejection. This stage determines the Op-Amp's input offset voltage, input bias current, and noise characteristics.**
2. **Intermediate Gain Stage(s): These stages provide additional voltage gain and often incorporate level shifting (to bring the signal reference to ground for single-ended output). They typically consist of common-emitter or common-collector configurations.**
3. **Output Stage: This is usually a Class AB push-pull amplifier (complementary symmetry) designed to provide low output impedance and sufficient current drive capability to the load. It ensures the Op-Amp can deliver power without significant distortion. It often includes current limiting to protect the Op-Amp from excessive load currents.**

4.2.2 Basic Op-Amp Gain Stages (with Negative Feedback)

Since the open-loop gain of an Op-Amp is extremely high and unstable, it is almost always used with negative feedback to control its gain and improve performance.

- **Ideal Op-Amp Assumptions (for simplified analysis):**
  - **No current flows into the input terminals (infinite input impedance).**
  - **The voltage difference between the inverting (-) and non-inverting (+) inputs is zero (virtual short circuit).**

4.2.2.1 Inverting Amplifier

- **Configuration: The input signal is applied to the inverting (-) input through an input resistor (R_in). The non-inverting (+) input is grounded. A feedback resistor (R_f) connects the output to the inverting input.**
- **Voltage Gain (A_v):**
  A_v=fracV_outV_in=−fracR_fR_in
  The negative sign indicates a 180-degree phase shift between input and output.
- **Input Impedance (Z_in): Approximately equal to R_in.**
- **Output Impedance (Z_out): Very low (ideally zero), thanks to negative feedback.**

Numerical Example (Inverting Amplifier):

If R_in=1kOmega and R_f=10kOmega.

A_v=−frac10kOmega1kOmega=−10

4.2.2.2 Non-Inverting Amplifier

- **Configuration: The input signal is applied directly to the non-inverting (+) input. A feedback network (R_1 and R_2) from the output to the inverting (-) input controls the gain. R_2 is connected from the inverting input to ground, and R_1 is connected between the output and the inverting input.**
- **Voltage Gain (A_v):**
  A_v=fracV_outV_in=1+fracR_1R_2
- **Input Impedance (Z_in): Very high (ideally infinite), significantly higher than the Op-Amp's open-loop input impedance due to feedback.**
- **Output Impedance (Z_out): Very low (ideally zero), due to feedback.**

Numerical Example (Non-Inverting Amplifier):

If R_1=9kOmega and R_2=1kOmega.

A_v=1+frac9kOmega1kOmega=1+9=10

4.2.3 Bandwidth of Op-Amp Gain Stages

- **Real Op-Amps have finite bandwidth. The gain starts to roll off at higher frequencies.**
- **Gain-Bandwidth Product (GBW): For a compensated Op-Amp, the product of its open-loop gain (A) and its bandwidth (BW) is approximately constant.**
  GBWapproxAtimesBW
  This means if you reduce the gain (by applying negative feedback), the bandwidth increases proportionally.
- **For the inverting and non-inverting configurations:**
  BW_f=fracGBW|A_v|
  Where BW_f is the bandwidth with feedback, and |A_v| is the magnitude of the closed-loop gain.

Numerical Example (Bandwidth):

An LM741 Op-Amp has a typical GBW of 1 MHz.

For an inverting or non-inverting amplifier with a gain of 10:

BW_f=frac1textMHz10=100textkHz

5.0 CIRCUIT DIAGRAMS:

Figure 7.1: BJT Differential Amplifier with Current Source (or Resistor)

```
+Vcc (e.g., +12V or +15V DC)
    |
    Rc1 (Collector Resistor)      Rc2 (Collector Resistor)
    |                         |
    C1 (Collector) ---------- C2 (Collector)
```

```
          |   /|\                       |   /|\
          B1 (Base) ---------------------- B2 (Base)
          | \|/                       | \|/
          E1 (Emitter) ----- E2 (Emitter)
          \     /
           \   /
            \ /
          Common Emitter Node
               |
               R_E_CS (Resistor for Current Source approximation)
               |
               NPN Transistor (Q3) for Current Source Base Biasing
               |
               R_B_CS1 (Base Resistor 1 for Q3)
               |
               +---- Base of Q3 ---- Emitter of Q3 ----- Isource (to common Emitter)
               |
               R_B_CS2 (Base Resistor 2 for Q3)
               |
              -Vee (e.g., -12V or -15V DC)

   Simpler Version (using large resistor for current source approximation):
          +Vcc
             |
             Rc1               Rc2
             |                 |
             C1 ----------------- C2
             |   /|\           |   /|\
    Vin1 --- B1     | ------------ B2 --- Vin2
             | \|/           | \|/
             E1 ----- E2 (Common Emitter Node)
             \     /
              \   /
               \ /
                |
                R_E (Large Emitter Resistor, e.g., 22k - 100k Ohm)
                |
             -Vee (e.g., -12V or -15V DC)

   For Common Mode Input: Vin1 = Vin2 = Vic
   For Differential Input: Vin1 = Vid/2, Vin2 = -Vid/2 (or apply Vid to Vin1 and ground Vin2
for single-ended differential input)

   Outputs: Vout1 (at C1), Vout2 (at C2)
```

Figure 7.2: Op-Amp Inverting Amplifier

```
          +Vcc (e.g., +15V)
            |
```

```
   Op-Amp (e.g., LM741)
Non-inverting Input (+) --- GND
                |
                +-- Rf (Feedback Resistor)
                |
Inverting Input (-) ---+
                |
                +-- Rin (Input Resistor) --- Vin (Input Signal)

Output of Op-Amp (Vout) --- (Connected to Rf)

    -Vcc (e.g., -15V)
```

Figure 7.3: Op-Amp Non-Inverting Amplifier

```
    +Vcc (e.g., +15V)
      |
   Op-Amp (e.g., LM741)
Non-inverting Input (+) --- Vin (Input Signal)
                |
                +-- R1 (Feedback Resistor)
                |
Inverting Input (-) ---+
                |
                +-- R2 (Feedback Resistor)
                |
                GND

Output of Op-Amp (Vout) --- (Connected to R1)

    -Vcc (e.g., -15V)
```

6.0 PROCEDURE:

Follow these systematic steps to design, build, and characterize the differential amplifier and Op-Amp gain stages.

Part A: BJT Differential Amplifier Characterization

1. **Differential Amplifier Design (DC Biasing):**
    - **Power Supply: Use a dual power supply (e.g., +/- 12V or +/- 15V).**
    - **Current Source Design:**
        - **Option 1 (Resistor Approximation): Select a large emitter resistor (R_E, e.g., 22 kΩ to 100 kΩ) connected from the common emitter node to the negative supply (-Vee). This provides a relatively constant current ($I_E \approx (-V_{EE} - V_{BE})/R_E$) shared by the two transistors.**

        - **Option 2 (Dedicated BJT Current Source - Recommended for better CMRR): Design a simple BJT current source circuit using a third NPN transistor (Q3) and two resistors to set its base voltage and emitter current. The collector of Q3 then connects to the common emitters of Q1 and Q2. (Refer to Figure 7.1, the more complex version). Target a total current (e.g., 1 mA or 2 mA) to be split equally between Q1 and Q2. So, $I_{CQ1}=I_{CQ2}=I_{total}/2$.**
    - **Collector Resistors (R_C): Choose R_C values (e.g., 4.7 kΩ to 10 kΩ) to achieve appropriate voltage drops and set collector voltages within the active region. Ensure $V_C - V_E \approx 1V$ for both transistors.**
    - **Transistor Matching: If possible, select two NPN BJTs (Q1 and Q2) with as similar beta (hFE) values as possible using a DMM.**
    - **Pre-Calculations: Calculate theoretical A_d, A_{cm} (if using R_E), and CMRR based on your design values. Record these in Table 7.1.**
2. **Circuit Construction:**
    - **Assemble the BJT differential amplifier on the breadboard as per Figure 7.1. Pay close attention to transistor pinouts and resistor values.**
3. **DC Q-point Measurement:**
    - **Apply the dual DC power supply.**
    - **Measure the DC voltages at the bases, emitters, and collectors of Q1 and Q2 using the DMM. Verify that both transistors are biased in the active region and that the current source is functioning as expected.**
    - **Measure the voltage across one of the collector resistors and calculate the approximate collector current for one side ($I_{CQ}=V_{RC}/R_C$). Record in Table 7.1.**
4. **Differential Gain (A_d) Measurement:**
    - **Apply a small sinusoidal input signal (V_{in}) (e.g., 100 mV p-p at 1 kHz) to the base of Q1 (V_{in1}) and ground the base of Q2 ($V_{in2}=0$). This forms a single-ended differential input.**
    - **Connect Oscilloscope Channel 1 to V_{in1} and Channel 2 to V_{out1} (collector of Q1).**
    - **Measure $V_{in(p-p)}$ and $V_{out(p-p)}$ from Channel 2.**
    - **Calculate $A_d=V_{out(p-p)}/V_{in(p-p)}$. Note the phase shift.**
    - **Alternatively, to measure true differential gain, apply V_{in} to V_{in1} and $-V_{in}$ (inverted signal from function generator or phase splitter) to V_{in2}. Or, apply $V_{in}/2$ to V_{in1} and $-V_{in}/2$ to V_{in2}. Then $A_d=V_{out}/(V_{in1}-V_{in2})$. The first method (one input driven, other grounded) is often sufficient for practical purposes, as $V_{id}=V_{in1}-0=V_{in1}$.**
    - **Record measured A_d in Table 7.2.**
5. **Common-Mode Gain (A_{cm}) Measurement:**
    - **Connect the bases of Q1 and Q2 together, and apply a sinusoidal input signal (V_{ic}) (e.g., 100 mV p-p at 1 kHz) to this common point.**
    - **Connect Oscilloscope Channel 1 to the common input (V_{ic}) and Channel 2 to V_{out1} (collector of Q1).**
    - **Measure $V_{ic(p-p)}$ and $V_{out(p-p)}$. Note that V_{out} should be very small.**

- **Calculate A_cm=V_out(p−p)/V_ic(p−p). Record measured A_cm in Table 7.2.**

6. **CMRR Calculation:**
   - **Using your measured A_d and A_cm from steps A.4 and A.5, calculate the Common Mode Rejection Ratio:**
     CMRR=|A_d|/|A_cm|
     CMRR_dB=20log_10(CMRR)
   - **Record in Table 7.2.**

Part B: Input Common Mode Range (ICMR) Determination

1. **Setup:**
   - **Keep the differential amplifier circuit from Part A.**
   - **Connect the bases of Q1 and Q2 together.**
   - **Apply a DC voltage source to this common base point (using a variable DC power supply or potentiometer connected to a fixed supply). Use the DMM to measure this common-mode DC input voltage (V_ic).**
   - **Connect the oscilloscope to V_out1 (collector of Q1) to monitor the output.**
   - **Superimpose a small AC signal (e.g., 1 kHz, 50 mV p-p) on this DC common-mode input voltage. This AC signal will allow you to see the gain.**
2. **Procedure:**
   - **Slowly vary the common-mode DC input voltage (V_ic) from a low negative value towards positive.**
   - **Observe the AC output signal on the oscilloscope.**
   - **Note the lowest common-mode input voltage at which the output signal starts to distort or disappear (indicating cutoff). This is your lower ICMR limit.**
   - **Note the highest common-mode input voltage at which the output signal starts to distort or clip (indicating saturation or cutoff at the upper rail). This is your upper ICMR limit.**
   - **Record these values in Table 7.3.**

Part C: Op-Amp Basic Gain Stages Characterization

1. **Op-Amp Power Supply: Connect the Op-Amp (LM741) to a dual DC power supply (e.g., +/- 15V). Pin 7 to +Vcc, Pin 4 to -Vee.**
2. **Inverting Amplifier:**
   - **Design: Choose values for R_in and R_f to achieve a desired gain (e.g., gain of -10: R_in=1kOmega, R_f=10kOmega).**
   - **Circuit Construction: Assemble the inverting amplifier circuit as per Figure 7.2. Ground the non-inverting input.**
   - **Gain Measurement: Apply a sinusoidal input signal (e.g., 1 kHz, 100 mV p-p) to R_in. Measure V_in(p−p) and V_out(p−p) using the oscilloscope. Calculate A_v=V_out/V_in. Observe the phase shift (should be 180 degrees). Record in Table 7.4.**

- **Bandwidth Measurement: Perform a frequency sweep (similar to Experiment 3, Part C). Keep V_in constant. Vary the frequency from mid-band (e.g., 1 kHz) upwards until the gain drops by 3 dB from the mid-band gain. This is your upper cutoff frequency (f_H). Since Op-Amp circuits typically have low-frequency gain maintained by coupling capacitors, f_L is usually very low. Calculate the bandwidth BW=f_H−f_Lapproxf_H. Record in Table 7.4.**

3. **Non-Inverting Amplifier:**
   - **Design: Choose values for R_1 and R_2 to achieve a desired gain (e.g., gain of +10: R_1=9kOmega or 8.2k+820k, R_2=1kOmega).**
   - **Circuit Construction: Assemble the non-inverting amplifier circuit as per Figure 7.3. Connect V_in directly to the non-inverting input.**
   - **Gain Measurement: Apply a sinusoidal input signal (e.g., 1 kHz, 100 mV p-p). Measure V_in(p−p) and V_out(p−p). Calculate A_v=V_out/V_in. Observe the phase (should be 0 degrees). Record in Table 7.4.**
   - **Bandwidth Measurement: Perform a frequency sweep similar to the inverting amplifier to find f_H. Calculate BW. Record in Table 7.4.**

Part D: Internal Op-Amp Stages (Conceptual/Discussion)

1. **Discussion: Based on the theoretical knowledge from Section 4.2.1 and your observations from Op-Amp circuits, discuss the roles of the three main internal stages of a typical Op-Amp.**
2. **Identification: For example, how does the differential input stage provide high input impedance and common-mode rejection? How do intermediate stages contribute to high gain? How does the output stage provide current driving capability and low output impedance? This part primarily involves analysis and discussion rather than direct measurement.**

7.0 OBSERVATIONS AND READINGS:

7.1 BJT Differential Amplifier DC Biasing and Design Parameters:

Parameter	Designed/Calculated Value	Measured Value	Remarks/Comparison
+Vcc (Supply Voltage)		_____ V	
-Vee (Supply Voltage)		_____ V	

R_C1	**_____ Ω**	**_____ Ω**	
R_C2	**_____ Ω**	**_____ Ω**	
Current Source Type	**(e.g., Resistor/BJT CS)**		
R_E (if resistor CS)	**_____ Ω**	**_____ Ω**	
Current Source Total Current (I_E)	**_____ mA**	**_____ mA**	
I_CQ1 (for Q1)	**_____ mA**	**_____ mA**	
I_CQ2 (for Q2)	**_____ mA**	**_____ mA**	
V_B1	**_____ V**	**_____ V**	
V_E1	**_____ V**	**_____ V**	
V_C1	**_____ V**	**_____ V**	

V_B2	**_____ V**	**_____ V**	
V_E2	**_____ V**	**_____ V**	
V_C2	**_____ V**	**_____ V**	

7.2 BJT Differential Amplifier AC Performance:

Parameter	**Theoretical Calculated Value**	**Measured Experimental Value**	**Remarks/Comparison**
A_d (Differential Gain)	**_____**	**_____**	
A_cm (Common-Mode Gain)	**_____**	**_____**	
CMRR (Ratio)	**_____**	**_____**	
CMRR (dB)	**_____ dB**	**_____ dB**	

7.3 Input Common Mode Range (ICMR) of Differential Amplifier:

Parameter	**Measured Value (Volts)**

Lower ICMR Limit	**_____ V**
Upper ICMR Limit	**_____ V**
ICMR Range	**_____ V to _____ V**

7.4 Op-Amp Basic Gain Stages Data:

- **Op-Amp Type: LM741**
- **Supply Voltages: +Vcc = _____ V, -Vee = _____ V**

Parameter	**Inverting Amplifier**	**Non-Inverting Amplifier**
Circuit Resistors:	**R_in = _____ Ω, R_f = _____ Ω**	**R_1 = _____ Ω, R_2 = _____ Ω**
Theoretical Gain (A_v):	**_____**	**_____**
Measured V_in(p−p):	**_____ V**	**_____ V**
Measured V_out(p−p):	**_____ V**	**_____ V**
Measured Gain (A_v):	**_____**	**_____**
Phase Shift (Input to Output):	**_____ degrees (e.g., 180)**	**_____ degrees (e.g., 0)**

Measured Bandwidth (BW):	**_____ Hz**	**_____ Hz**

8.0 GRAPHS:

Include relevant graphs based on your experimental data. Use appropriate labels and scales.

- **Graph 7.1: ICMR Determination Plot (Optional but Recommended for Clarity)**
  - **Type: Linear plot.**
  - **Plot: Plot Output AC voltage (Y-axis) vs. DC Common Mode Input Voltage (X-axis).**
  - **Markings: Clearly mark the linear operating region and the points where distortion or clipping begins, indicating the lower and upper ICMR limits.**
- **Graph 7.2: Frequency Response of Op-Amp Inverting Amplifier**
  - **Type: Semi-log graph (logarithmic X-axis for frequency, linear Y-axis for gain in dB).**
  - **Plot: Plot Gain in dB (Y-axis) versus Frequency (X-axis).**
  - **Markings: Clearly mark the mid-band gain and the -3 dB cutoff frequency (f_H).**
- **Graph 7.3: Frequency Response of Op-Amp Non-Inverting Amplifier**
  - **Type: Semi-log graph (logarithmic X-axis for frequency, linear Y-axis for gain in dB).**
  - **Plot: Plot Gain in dB (Y-axis) versus Frequency (X-axis).**
  - **Markings: Clearly mark the mid-band gain and the -3 dB cutoff frequency (f_H).**

9.0 CALCULATIONS:

Provide detailed steps for all calculations performed in this experiment, using your measured values where appropriate.

9.1 BJT Differential Amplifier Calculations:

- **For Differential Gain (A_d):**
  - **Calculate I_CQ (quiescent collector current per transistor, from 7.1).**
  - **Calculate Transconductance (g_m=I_CQ/V_T, where V_T=26textmV).**
  - **A_d=−fracg_mR_C2 = [Your Calculation]**
- **For Common-Mode Gain (A_cm):**
  - **If using resistor R_E for current source: A_cm=−fracR_C2R_E = [Your Calculation]**
  - **If using BJT current source: (This formula is more complex, involving output resistance of current source, r_o. Often, A_cm is primarily determined experimentally due to high output resistance.)**

- **For CMRR:**
    - **CMRR=frac∣A_d∣∣A_cm∣ (using measured values from 7.2) = [Your Calculation]**
    - **CMRR_dB=20log_10(CMRR) = [Your Calculation] dB**

9.2 Op-Amp Basic Gain Stages Calculations:

- **For Inverting Amplifier:**
    - **Theoretical Gain (A_v) = −fracR_fR_in = [Your Calculation]**
    - **Measured Gain (A_v) = fracV_out(p−p)V_in(p−p) = [Your Calculation]**
    - **Calculated Bandwidth (BW) based on LM741 GBW (1 MHz typical): BW=fracGBW∣A_v∣ = [Your Calculation] Hz**
- **For Non-Inverting Amplifier:**
    - **Theoretical Gain (A_v) = 1+fracR_1R_2 = [Your Calculation]**
    - **Measured Gain (A_v) = fracV_out(p−p)V_in(p−p) = [Your Calculation]**
    - **Calculated Bandwidth (BW) based on LM741 GBW (1 MHz typical): BW=fracGBW∣A_v∣ = [Your Calculation] Hz**

10.0 RESULTS:

Present the significant numerical results obtained from the experiment in a clear and concise manner.

- **BJT Differential Amplifier:**
    - **Measured Differential Gain (A_d): [Your Value]**
    - **Measured Common-Mode Gain (A_cm): [Your Value]**
    - **Calculated Common Mode Rejection Ratio (CMRR): [Your Value] dB**
    - **Determined Input Common Mode Range (ICMR): [Lower Limit] V to [Upper Limit] V**
- **Op-Amp Inverting Amplifier:**
    - **Measured Voltage Gain (A_v): [Your Value]**
    - **Measured Bandwidth (BW): [Your Value] Hz**
- **Op-Amp Non-Inverting Amplifier:**
    - **Measured Voltage Gain (A_v): [Your Value]**
    - **Measured Bandwidth (BW): [Your Value] Hz**

11.0 DISCUSSION AND ANALYSIS:

This is the most critical section where you interpret your results, compare them with theoretical expectations, explain observed phenomena, and discuss any discrepancies.

1. **BJT Differential Amplifier Performance:**
    - **DC Biasing: Discuss whether the measured DC operating points (Q-points) of Q1 and Q2 were balanced and within the active region.**

Comment on the effectiveness of your chosen current source (or R_E approximation) in setting the total emitter current.

- **Differential Gain (A_d): Compare your measured A_d with the theoretically calculated value. Discuss any differences and potential reasons (e.g., transistor mismatch, variation in actual V_T, measurement inaccuracies, loading effects). Explain the significance of the phase shift observed.**
- **Common-Mode Gain (A_cm): Discuss your measured A_cm. Was it small, as expected? Explain why a differential amplifier ideally produces a very small output for common-mode input signals. What aspects of the circuit (e.g., matched transistors, ideal current source) contribute to a low A_cm?**
- **Common Mode Rejection Ratio (CMRR): Analyze your calculated CMRR. Is it high? Explain the importance of a high CMRR in practical applications (e.g., rejecting noise picked up on signal lines, amplifying small differential signals in the presence of large common-mode noise). How do mismatches in transistors or collector resistors affect CMRR? How would using a more ideal current source improve CMRR?**
- **Input Common Mode Range (ICMR): Discuss the determined ICMR. How did the output waveform behave when the common-mode input voltage went beyond these limits? Explain the physical reasons (transistor cutoff or saturation) for the ICMR limits. Why is understanding ICMR important in practical circuit design?**

2. **Op-Amp Basic Gain Stages:**
   - **Inverting vs. Non-Inverting Amplifier: Compare the measured voltage gains of the inverting and non-inverting amplifier configurations with their theoretically calculated values. Discuss the accuracy of the simple gain formulas. Explain the phase relationship observed for each configuration.**
   - **Input and Output Impedance (Qualitative): Based on the theoretical characteristics of Op-Amps with negative feedback, qualitatively discuss the expected high input impedance of the non-inverting amplifier and the relatively lower input impedance of the inverting amplifier. Also, discuss the very low output impedance of both configurations due to negative feedback.**
   - **Bandwidth Analysis: Compare the measured bandwidths of the inverting and non-inverting amplifiers. Did they roughly follow the relationship $BW = GBW / |A_v|$? Explain the concept of the Gain-Bandwidth Product (GBW) and its significance for Op-Amp performance. How does choosing a higher gain for an Op-Amp stage affect its bandwidth?**
3. **Internal Op-Amp Stages (Conceptual):**
   - **Role of Differential Input Stage: Discuss how the first stage of an Op-Amp (the differential amplifier) enables its primary function of amplifying differential signals while rejecting common-mode signals. How does it contribute to the Op-Amp's high input impedance and low input offset voltage?**

- **Role of Intermediate Gain Stages: Explain the function of the intermediate gain stages in an Op-Amp. How do they provide the very high open-loop voltage gain?**
- **Role of Output Stage: Describe the purpose of the output stage (typically Class AB). How does it allow the Op-Amp to drive a load with significant current, despite the input stages operating at very low currents? Why is it crucial for low output impedance?**

4. **Sources of Error and Limitations:**
   - **Identify potential sources of experimental error (e.g., component tolerances, non-ideal Op-Amp characteristics like finite input impedance, offset voltage, bias current, slew rate; transistor mismatch for differential amplifier; measurement inaccuracies of DMM and oscilloscope).**
   - **Discuss how these errors might lead to discrepancies between theoretical calculations and experimental measurements.**
   - **Comment on the limitations of simple theoretical models for real-world components. For example, how does the assumption of "ideal" Op-Amp inputs affect gain calculations, especially at high frequencies or high gains?**

12.0 CONCLUSION:

Conclude your experiment by summarizing the key learning outcomes and reinforcing the understanding gained.

This experiment provided an insightful exploration into two fundamental building blocks of analog electronics: the differential amplifier and the operational amplifier. We successfully constructed and characterized a BJT differential amplifier, quantitatively measuring its differential gain, common-mode gain, and importantly, its Common Mode Rejection Ratio (CMRR), demonstrating its ability to discriminate between differential and common-mode signals. The determination of the Input Common Mode Range (ICMR) highlighted the practical limits of its linear operation. Furthermore, the experiment offered practical experience in implementing and characterizing basic Op-Amp gain stages (inverting and non-inverting configurations), confirming their predictable voltage gains and the gain-bandwidth trade-off. Through conceptual discussion, we gained a deeper understanding of the internal multi-stage architecture of a typical Op-Amp. Overall, this experiment has provided a strong foundation for understanding the principles and applications of differential amplification and the versatility of operational amplifiers in various electronic circuit designs.
